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2012 Programming weather, climate, and earth-system models on heterogeneous multi-core platforms

September 12-13, 2012 at the National Center for Atmospheric Research in Boulder, Colorado

Addressing the Increasing Challenges of Debugging on Accelerated Multi-Core Systems

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Senior Sales Engineer

Agenda

Overview - Rogue Wave & TotalView

Heterogeneous Systems - Then and Now

Debugging Accelerated Systems

GPU - Nvdia CUDA

MIC - Intel Phi

Rogue Wave Today

The largest independent provider of cross-platform software development tools and embedded components for the next generation of HPC applications

Leader in embeddable math and statistics algorithms and visualization software for data-intensive applications.

Leading provider of intelligent software technology which analyzes and optimizes computing performance in single and multi-core environments.

Industry-leading interactive analysis and debugging tools for the world's most sophisticated software applications.

Latest addition to the Rogue Wave family: <u>Rogue Wave Visualization for C++</u> (Formerly IBM's ILOG <u>Visualization for C++</u> products)
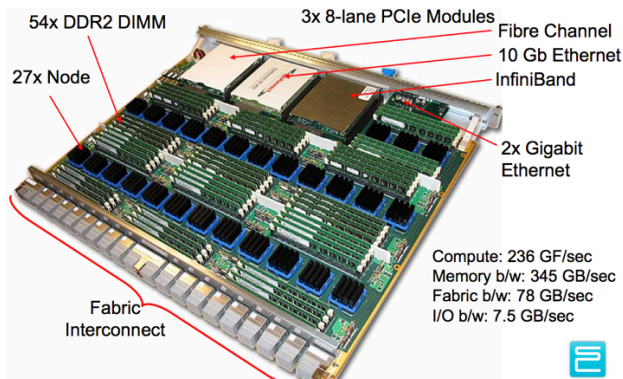
3

Representative Customers

Heterogeneous Systems and the Need for Speed
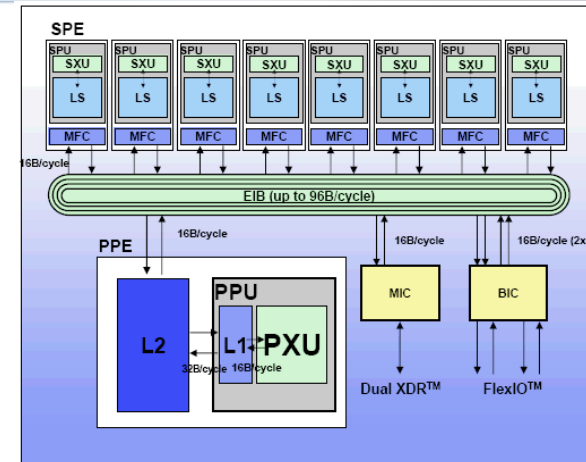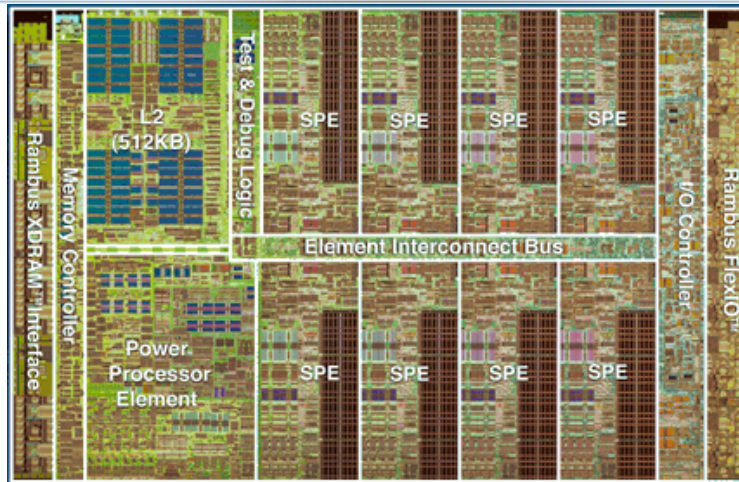
A couple of pioneers

Remember SiCortex?

Heterogeneous Systems - SiCortex   2003 - May 2009

27-Node Module

54x DDR2 DIMM   3x 8-lane PCIe Modules
27x Node
Fibre Channel
10 Gb Ethernet
InfiniBand
2x Gigabit Ethernet

Fabric Interconnect

Compute: 236 GF/sec
Memory b/w: 345 GB/sec
Fabric b/w: 78 GB/sec
I/O b/w: 7.5 GB/sec

14

SiCortex

SC648

An X-86 host with up to 972 MIPS nodes, with up to 5,832 cores and 7,776 GB of memory

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Remember Cell?

Source: M. Gschwind et al., Hot Chips-17, August 2005

RoadRunner

a hybrid design with 12,960 IBM PowerXCell 8i and 6,480 AMD Opteron dual-core processors

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What is TotalView?

A comprehensive debugging solution for demanding parallel, heterogeneous, and multi-core applications

- **Wide compiler & platform support**
  - C, C++, Fortran 77 & 90, UPC
  - Unix, Linux, OS X

- **Handles Concurrency**
  - Multi-threaded Debugging
  - Multi-process Debugging

- **Integrated Memory Debugging**

- **Reverse Debugging for Linux**

- **Supports Multiple Usage Models**
  - Powerful and Easy GUI – Highly Graphical
  - CLI for Scripting
  - Long Distance Remote Debugging
  - Unattended Batch Debugging

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GPU Debugging

with

TotalView

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CUDA Port of TotalView

Full visibility of both Linux and GPU threads

Device threads shown as part of the parent Unix process
Handles all the differences between the CPU and GPU

Fully represent the hierarchical memory

Display data at any level (registers, local, block, global or host memory)
Making it clear where data resides with type qualification

Thread and Block Coordinates

Built in runtime variables display threads in a warp, block and thread dimensions and indexes
Displayed on the interface in the status bar, thread tab and stack frame

Device thread control

Warps advance synchronously

Handles CUDA function inlining

Step into or over inlined functions
Functions show on stack trace

Reports memory access errors

CUDA memcheck

Multi-Device Support

Can be used with MPI

Starting TotalView

- **Once a new kernel is loaded TotalView provides the option to stop and set breakpoints**

- **TotalView automatically configures the GUI for CUDA debugging**

- **Debugging CUDA code is done by using normal TotalView commands and procedures**

GPU Device Status Display

Provides the "high-level" view

- **Values automatically update as you step through code**

- **Shows what hardware is in use**

- **Helps to map between logical and hardware coordinates**

Name	Description
Device 0/3	
—Device Type	gf100
—Lanes	32
SM 2/1	
—Valid Warps	0000000000000001
Warp 00/48	Block (0,0,0)
Lane 00/32	Thread (0,0,0)
└PC	0000000019aa94d8
Lane 01/32	Thread (1,0,0)
└PC	0000000019aa94d8
Lane 02/32	Thread (2,0,0)
└PC	0000000019aa94f0
Lane 03/32	Thread (3,0,0)
└PC	0000000019aa94f0
Lane 04/32	Thread (4,0,0)
└PC	0000000019aa94f0
Lane 05/32	Thread (5,0,0)
└PC	0000000019aa94f0
Lane 06/32	Thread (6,0,0)
└PC	0000000019aa94f0
Lane 07/32	Thread (7,0,0)
└PC	0000000019aa94f0
Lane 08/32	Thread (8,0,0)
└PC	0000000019aa94f0
Lane 09/32	Thread (9,0,0)
└PC	0000000019aa94f0
—Valid/Active/Divergent	000003ff, 000003fc, 00000003
—SM Type	sm_20
—SMs	14
—Warps	48
Device 1/3	
—Device Type	gt200
—Lanes	32
—SM Type	sm_13

GPU Device Status Display

Provides detailed information for:

Device and Type

SMs

Warps

Lanes with PC

Information updates as you step

Name	Descr
⊞-Device 0/3	
─Device Type	gf100
─Lanes	32
⊞-SM 2/1	
─Valid Warps	000000
⊞-Warp 00/48	Block
⊞-Lane 00/32	Thread
└PC	000000
⊞-Lane 01/32	Thread
└PC	000000
⊞-Lane 02/32	Thread
└PC	000000
⊞-Lane 03/32	Thread
└PC	000000
⊞-Lane 04/32	Thread
└PC	000000
⊞-Lane 05/32	Thread

GPU Device Status Display

```
Name                    Description
⊞-Device 0/3
  ─Device Type          gf100
  ─Lanes                32
  ⊞-SM 2/1
    ─Valid Warps        0000000000000001
    ⊞-Warp 00/48        Block (0,0,0)
      ⊞─Lane 00/32      Thread (0,0,0)
        └PC             0000000019aa94d8
      ⊞─Lane 01/32      Thread (1,0,0)
        └PC             0000000019aa94d8
      ⊞─Lane 02/32      Thread (2,0,0)
        └PC             0000000019aa94f0
      ⊞─Lane 03/32      Thread (3,0,0)
        └PC             0000000019aa94f0
      ⊞─Lane 04/32      Thread (4,0,0)
        └PC             0000000019aa94f0
      ⊞─Lane 05/32      Thread (5,0,0)
        └PC             0000000019aa94f0
      ⊞─Lane 06/32      Thread (6,0,0)
        └PC             0000000019aa94f0
      ⊞─Lane 07/32      Thread (7,0,0)
        └PC             0000000019aa94f0
      ⊞─Lane 08/32      Thread (8,0,0)
        └PC             0000000019aa94f0
      ⊞─Lane 09/32      Thread (9,0,0)
        └PC             0000000019aa94f0
      └Valid/Active/Divergent 000003ff, 000003fc, 00000003
  ─SM Type              sm_20
  ─SMs                  14
  └Warps                48
⊞-Device 1/3
  ─Device Type          gt200
  ─Lanes                32
  ─SM Type              sm_13
```

It also provides information for divergent GPU threads

Different PC for two groups of Lanes

State of Lanes inside the Warp

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Debugging CUDA

**Information on GPU execution, location and data is readily available.
... the same as it is for Linux processes and threads.**

Debugging CUDA

CUDA grid and block dimensions, lanes/ warp, warps/SM,

Parameter, register, local and shared variables

Debugging CUDA

GPU focus thread logical coordinates in the header...

Debugging CUDA

```
87   // Matrix multiplication kernel called by Matr
88   __global__ void MatMulKernel(Matrix A, Matrix
89   {
90       // Block row and column
91       int blockRow = blockIdx.y;
92       int blockCol = blockIdx.x;
93       // Each thread block computes one sub-matrix
⇨        Matrix Csub = GetSubMatrix(C, blockRow, bloc
95       // Each thread computes one element of Csub
96       // by accumulating results into Cvalue
97       float Cvalue = 0;
98       // Thread row and column within Csub
99       int row = threadIdx.y;
100      int col = threadIdx.x;
101      // Loop over all the sub-matrices of A and B
```

Action Points | **Processes** | **Threads**

```
1.1    (4735070203624 0)  T        in cudbgApiInit
1.2        (1095072064)  T        in __select_nocancel
1.-1  ((0,0,0)(1,1,0))  B1       in MatMulKernel
```

... as well as in the Process Window

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Debugging CUDA

PC arrow shows the Program Counter for the warp

```
Thread -1 (<<<(0,0,0),(1,1,0)>>>). @TEMP @CUDA@:A_c
```

Stack Trace

| C++ | MatMulKernel, | FP=fffca0 |

```
Function "M
    Device:
    SM/WP/LN:
    A:
    B:
    C:
Block "$b1#
    Csub:
    blockRow:
    blockCol:
    Cvalue:
```

Function MatMulKernel in tx_cuda_ma

```
84      cudaFree(d_C.elements);
85  }
86
87  // Matrix multiplication kernel called by MatrixMul
88  __global__ void MatMulKernel(Matrix A, Matrix B, Mat
89  {
90      // Block row and column
91      int blockRow = blockIdx.y;
92      int blockCol = blockIdx.x;
93      // Each thread block computes one sub-matrix Csub
⇒94     Matrix Csub = GetSubMatrix(C, blockRow, blockCol)
95      // Each thread computes one element of Csub
96      // by accumulating results into Cvalue
97      float Cvalue = 0;
98      // Thread row and column within Csub
99      int row = threadIdx.y;
100     int col = threadIdx.x;
101     // Loop over all the sub-matrices of A and B that
```

Action Points | Processes | Threads

```
1.1     (47350702036240)    T       in cudbgApiInit
1.2         (1095072064)    T       in __select_nocancel
1.-1    ((0,0,0) (1,1,0))   B1      in MatMulKernel
```

Debugging CUDA

Dive on any variable name to open a variable window

Debugging CUDA

A - MatMulKernel - 1.-1

File Edit View Tools Window   Help

1.-1

Expression: A   Address: 0x00000010
Type: @parameter const Matrix

Field	Type	Value
width	int	0x00000002 (2)
height	int	0x00000002 (2)
stride	int	0x00000002 (2)
elements	float @global *	0x00110000 -> 0

"@parameter" type qualifier indicates that variable "A" is in parameter storage

Address 0x10 is an offset within parameter storage

Pointer value 0x110000 is an offset within global storage

"elements" is a pointer to a float in global storage

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Storage Qualifiers

- **Denotes location in hierarchical memory**
  - **Part of the type – using "@" notation**
  - **Each memory space has a separate address space so 0x00001234 could refer to several places**

Storage Qualifier	Meaning
@parameter	Address is an offset within parameter storage.
@local	Address is an offset within local storage.
@shared	Address is an offset within shared storage.
@constant	Address is an offset within constant storage.
@global	Address is an offset within global storage.
@register	Address is a PTX register name

File	Edit	View	Tools	Window		Help

1.-1

Expression: Bsub   Address: 0x00000120
Type: @local Matrix

Field	Type	Value	
width	int	0x00000002 (2)	
height	int	0x00000002 (2)	
stride	int	0x00000014 (20)	
elements	float @global *	0x00111310 -> 4	

File	Edit	View	Window

1.-1

Expression	Type	Value	
Bs[row][col]	float	812	0x0000
row	@register int	0x00000000 (0)	%r31
col	@register int	0x00000000 (0)	%r33
Bs[1][0]	float	832	0x0000
Bs[row+1][1]	float	833	0x0000
row+1	@register int	0x00000001 (1)	(None)
A	@parameter const Matrix	(Matrix const @parameter)	0x0000
Asub	@local Matrix	(Matrix @local)	0x0000
*(Asub.elements)	@global float	20	0x0011

- **Used throughout expression system**
  - **You can cast to switch between different spaces**

Debugging CUDA - Navigation

Navigate through your CUDA code in the Process Window as you wish...
Using either of two coordinate systems:

Debugging CUDA - Navigation

CUDA GPU threads have a negative TotalView thread ID

Block (x,y,z)

Thread (x,y,z)

User-controlled "spinboxes" allow selection and display of any part of your GPU execution

GPU focus thread selector for changing the logical block and thread indexes of the CUDA thread.

- Logical: 2 or 3D Grid of Blocks, 3D Thread Within Grid

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Debugging CUDA - Navigation

Device, SM, Warp, and Lane

User-controlled "spinboxes" allow selection and display of any part of your GPU execution

GPU focus selector for changing physical indexes of the CUDA thread.

- **Physical: Device, SM, Warp, Lane**

Executing GPU Code - Threads and Warps

- **Single-step operation advances all of the GPU hardware threads in the *same* warp**

- **To advance the execution of more than one warp:**
  - **set a breakpoint and continue the process, or**
  - **select a line number in the source pane and select "Run To".**

- **Warps advance synchronously**
  - **Warps share a PC**

- **Single stepping**
  - **Advances the warp containing the focus thread**
  - **Stepping over a __syncthreads() call advances all the relevant threads**

- **Continue and runto**
  - **Continues more than just the warp**

- **Halt**
  - **Stops all the host and device threads**

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CUDA Segmentation Faults

- **TotalView displays segmentation faults as expected**
  - **Enable CUDA memory checking in New Program dialog window**

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What's New

Intel Phi Debugging

with

TotalView

A Spectrum of Programming Use Models

Xeon-Centric   MIC-Centric

Xeon-native   Offload   Symmetric   Reverse Offload   MIC-native

General Purpose Serial and Parallel Codes

Codes with balanced needs

Highly parallel codes

Main()
MPI_
Foo()

Scalar codes with highly parallel phases

Main()
Foo()

Main()
Foo()

Parallel codes with scalar phases

Main()
MPI_
Foo()

Main()
----
offload<MIC>
Foo()

Main()

Offload<Xeon>
Foo()

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Intel MIC Port of TotalView

- **Full visibility of both host and Phi threads**

- **Full support of MPI programs**

- **Symmetric Debugging of heterogeneous applications with offloaded code**

- **Remote Debugging of Phi-native applications**

- **Asynchronous thread control on both Xeon and Phi**

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Debugging MPI Applications

- **Attach to subset of processes on Phi**

- **Set breakpoints**
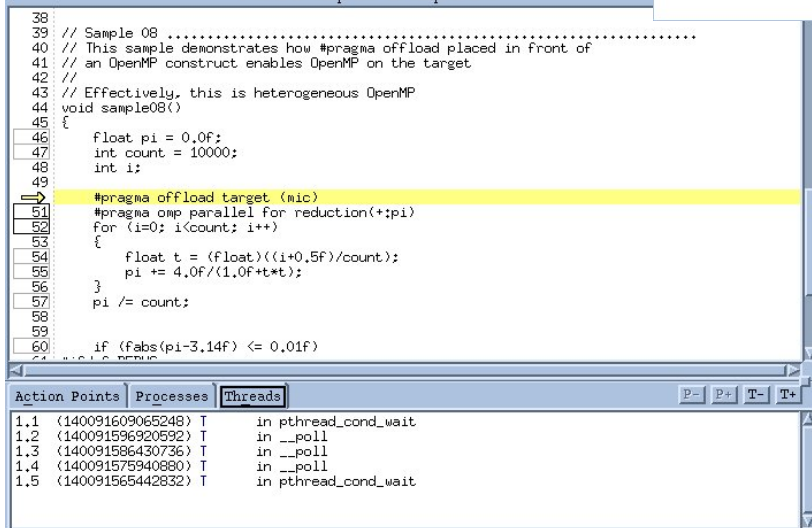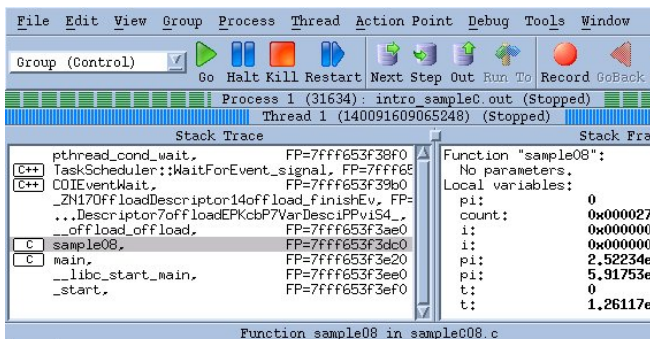
- **Debug MPI "as usual"**

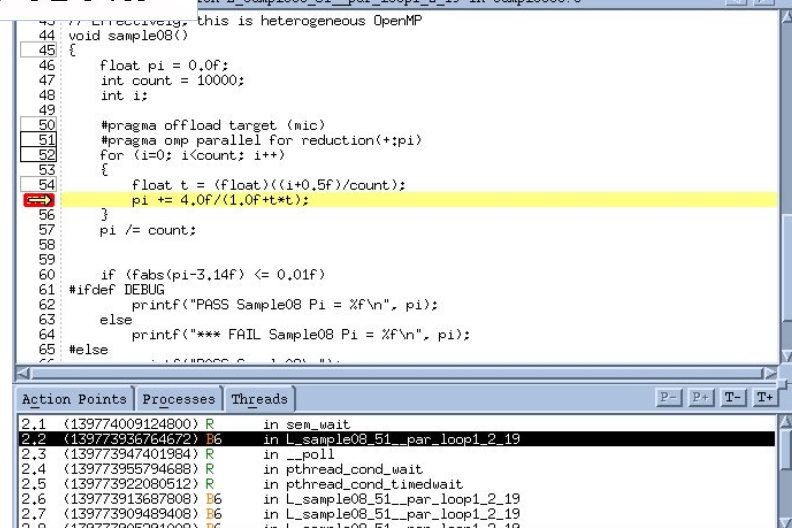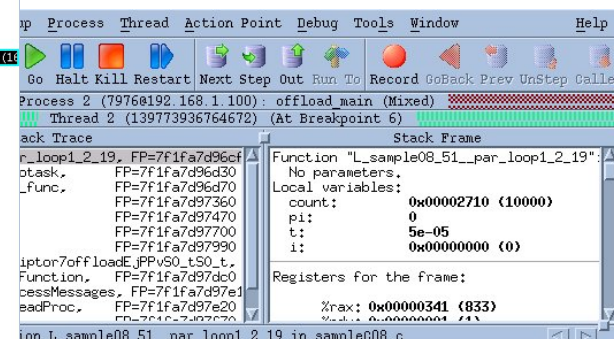# Remote Debugging of Applications on Phi

- **Start application on Phi card**

- **Attach to running application**

- **See thread private data**

- **Investigate individual threads**

- **Kill stuck processes on Phi**

Debugging Applications with Offloaded Code

Xeon side

Phi side

One debugging session for Phi-accelerated code

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TotalView provides a <u>full spectrum</u> of debugging solutions

TotalView®

Code debugging
- **Highly scalable interactive GUI debugger**
  - Easy to use -- without sacrificing detail that users need to debug
  - Used from workstations to the largest supercomputers
- **Powerful features for debugging multi-threaded, multi-process, and MPI parallel programs**
- **Compatible with wide variety of compilers across several platforms and operating systems**

Memory Debugging
- **Parallel memory analysis and error detection**
  - Intuitive for both intensive and infrequent users
- **Easily integrated into the validation process**

Reverse Debugging
- **Parallel record and deterministic replay within TotalView**
  - Users can run their program "backwards" to find bugs
- **Allows straightforward resolution of otherwise stochastic bugs**

GPU CUDA Debugging
- **Full Hybrid Architecture Support**
- **Asynchronous Warp Control**
- **Multi-Device and MPI Support**

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Thanks!

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Thank You

Download a TotalView evaluation at:
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